IN THE CLAIMS:

1. (currently amended) A vector controller for a polyphase synchronous rectifier, comprising:

an input line voltage detector configured to detect voltages on at least two rectifier input lines and produce therefrom a neutral excursion vector;

an input line current detector configured to detect currents on at least two of said rectifier input lines and produce therefrom an uncompensated drive vector; and

a neutral excursion compensator, coupled to said input line voltage detector and said input line current detector, that applies said neutral excursion vector to a partially compensated drive vector to yield an excursion-compensated drive vector suitable for generation of excursion-compensated pulse-width modulated drive signals for said synchronous rectifier.

Claim 2 (canceled)

3. (currently amended) The controller as recited in Claim 1 ~~2~~ further comprising:

an output voltage detector configured to detect a bus voltage of said synchronous rectifier and produce therefrom a DC bus voltage; and

a current control block, coupled to said output voltage detector, that applies a reference current vector based on said DC bus voltage to said uncompensated drive vector to yield said partially compensated drive vector.

4. (original) The controller as recited in Claim 1 further comprising a zero-crossing detector configured to detect a phase on one of said at least two rectifier input lines and produce therefrom a zero-crossing signal for said input line voltage detector.

5. (original) The controller as recited in Claim 4 wherein said zero-crossing detector further provides said zero-crossing signal for an input line current detector.

6. (original) The controller as recited in Claim 1 further comprising a 2-3 transform that transforms said excursion-compensated drive vector into signals suitable for a pulse-width modulated drive signal generator.

7. (original) The controller as recited in Claim 1 further comprising a pulse-width modulated drive signal generator configured to generate said excursion-compensated pulse-width modulated drive signals for said synchronous rectifier.

8. (currently amended) A method of vector-controlling a polyphase synchronous rectifier, comprising:

detecting voltages on at least two rectifier input lines;

producing therefrom a neutral excursion vector;

detecting currents on at least two of said rectifier input lines;

producing therefrom an uncompensated drive vector; and

applying said neutral excursion vector to a partially compensated drive vector to yield an excursion-compensated drive vector suitable for generation of excursion-compensated pulse-width modulated drive signals for said synchronous rectifier.

Claim 9 (canceled)

10. (currently amended) The method as recited in Claim 8 ~~9~~ further comprising:

detecting a bus voltage of said synchronous rectifier;

producing therefrom a DC bus voltage vector; and

applying a reference current vector based on said DC bus voltage to said uncompensated drive vector to yield said partially compensated drive vector.

11. (original) The method as recited in Claim 8 further comprising:

detecting a phase on one of said at least two rectifier input lines; and

producing therefrom a zero-crossing signal for said input line voltage detector.

12. (original) The method as recited in Claim 11 further comprising further providing said zero-crossing signal for an input line current detector.

13. (original) The method as recited in Claim 8 further comprising transforming said excursion-compensated drive vector into signals suitable for a pulse-width modulated drive signal generator.

14. (original) The method as recited in Claim 8 further comprising generating said excursion-compensated pulse-width modulated drive signals for said synchronous rectifier.

15. (currently amended) A three-phase synchronous rectifier, comprising:

a plurality of power switches interposing three rectifier input lines and two rectifier output lines; and

a vector controller, including:

an input line voltage detector configured to detect voltages on at least two of said rectifier input lines and produce therefrom a neutral excursion vector,

an input line current detector configured to detect currents on at least two of said rectifier input lines and produce therefrom an uncompensated drive vector,

a neutral excursion compensator, coupled to said input line voltage detector and said input line current detector, that applies said neutral excursion vector to a partially compensated drive vector to yield an excursion-compensated drive vector, and

a pulse-width modulated drive signal generator configured to produce excursion-compensated pulse-width modulated drive signals from said excursion-compensated drive vector and drive said plurality of drive switches based thereon.

Claim 16 (canceled)

17. (currently amended) The synchronous rectifier as recited in Claim 15 ~~16~~ further comprising:

an output voltage detector configured to detect a bus voltage across said two rectifier output lines and produce therefrom a DC bus voltage; and

a current control block, coupled to said output voltage detector, that applies a reference current vector based on said DC bus voltage to said uncompensated drive vector to yield said partially compensated drive vector.

18. (original) The synchronous rectifier as recited in Claim 15 further comprising a zero-crossing detector configured to detect a phase on one of said three rectifier input lines and produce therefrom a zero-crossing signal for said input line voltage detector.

19. (original) The synchronous rectifier as recited in Claim 18 wherein said zero-crossing detector further provides said zero-crossing signal for an input line current detector.

20. (original) The synchronous rectifier as recited in Claim 15 further comprising a 2-3 transform that transforms said excursion-compensated drive vector into signals suitable for said pulse-width modulated drive signal generator.